CLAIMS

What is claimed is:

1. A data-input array comprising:

a maximum of N*(N-1)/2 input elements arranged in a matrix;

a plurality of N input/output (I/O) lines for transferring signals used to scan said matrix to determine which of said input elements is activated, wherein said plurality of N I/O lines are coupled to said input elements to create a plurality of signal paths, each of which uniquely couple two of said plurality of N I/O lines through an associated input element.

2. The data-input array of Claim 1, further comprising:

a plurality of pull down resistors for pulling said plurality of N I/O lines to a logic low level.

3. The data-input array of Claim 1, further comprising:

a plurality of pull up resistors for pulling said plurality of N I/O lines to a logic high level.

4. The data-input array of Claim 1, wherein at least one of said plurality of input elements comprises a switch.

5. The data-input array of Claim 2, wherein at least one of said plurality of pull down resistors comprises an active pull down resistor.

6. The data-input array of Claim 2, wherein at least one of said plurality of pull down resistors comprises a passive pull down resistor.

7. The data-input array of Claim 1, further comprising:

a system controller for scanning said matrix by sending a signal to said matrix from one of said plurality of N I/O lines and reading said signal at another of said plurality of N I/O lines when an activated input element completes a circuit path for said signal to return to said system controller.

8. The data-input array of Claim 1, wherein said data-input array comprises an N*N matrix that is configured to support said maximum of N*(N-1)/2 input elements.

9. The data-input array of Claim 1, wherein at least one of said plurality of N I/O lines is bi-directional, such that an associated signal comprises an input signal or an output signal.

10. The data-input array of Claim 1, wherein said signals comprises digital signals.

11. A data-input array comprising:

a maximum of N*(N-1) input elements arranged in a matrix;

a plurality of N input/output (I/O) lines for transferring signals used to scan said matrix to determine which of said input elements is activated, wherein said plurality of N I/O lines are coupled to said input elements to create a plurality of signal paths, each of which couple two of said plurality of N I/O lines through an associated input element; and

a plurality of diodes arranged to differentiate between pairs of input elements that complete paths between same pairs of said plurality of I/O lines when scanning said matrix.

12. The data-input array of Claim 11, wherein at least one of said plurality of input elements comprises a switch.

13. The data-input array of Claim 11, further comprising:

a plurality of pull down resistors for pulling said plurality of N I/O lines to a logic low level.

14. The data-input array of Claim 11, further comprising:

a plurality of pull up resistors for pulling said plurality of N I/O lines to a logic high level.

15. The data-input array of Claim 14, wherein at least one of said plurality of pull up resistors comprises an active pull up resistor.

16. The data-input array of Claim 14, wherein at least one of said plurality of pull up resistors comprises a passive pull up resistor.

17. The data-input array of Claim 11, further comprising:

a system controller for scanning said matrix by sending a signal to said matrix from one of said plurality of N I/O lines and reading said signal at another of said plurality of N I/O lines when an activated input element completes a circuit path for said signal to return to said system controller.

18. The data-input array of Claim 11, further comprising:

a pair of input elements;

a pair of I/O lines coupled to said pair of input elements for inputting a signal into one of said pair of I/O

lines and for reading said signal at another of said pair of I/O lines when one of said pair of input elements is activated; and

a pair of diodes coupled to said pair of I/O lines for differentiating which of said pair of input elements is activated when reading said signal at said another of said pair of I/O lines.

19. The data-input array of Claim 11, wherein said data-input array comprises an N*N matrix that is configured to support said maximum of N*(N-1) input elements.

20. The data-input array of Claim 11, wherein at least one of said plurality of N I/O lines is bi-directional, such that an associated signal comprises an input signal or an output signal.

21. The data-input array of Claim 11, wherein said data-input array is configured so that between any pair of I/O lines two circuit paths exist, each defining a unique switch and a unique passive device, wherein said unique passive device differentiates between said two circuit paths.

22. The data-input array of Claim 11, wherein said signals comprise digital signals.

23. The data-input array of Claim 11, wherein said signals comprise analog signals.

24. An electronic system configured to receive inputs, comprising:

a switch array comprising a maximum of N(N-1) switches;

a plurality of N input/output (I/O) lines coupled to said switch array for delivering digital signals through said system to scan said switch array;

a plurality of N passive devices configured to differentiate between pairs of said switches that complete similar circuit paths between pairs of I/O lines; and

a system controller coupled to said plurality of N I/O lines for scanning said switch array by sending said digital signals to said switch array from said N I/O lines and detecting said digital signals at said N I/O lines, wherein said switch array is configured so that between any pair of I/O lines two circuit paths exist, each defining a unique switch and passive device combination so that said system controller can differentiate between said two circuit paths.

25. The system of Claim 24, wherein said data-input array comprises an N*N matrix that is configured to support said maximum of N*(N-1) switches.

26. The system of Claim 24, wherein said data-input array comprises a keypad.

27. The system of Claim 24, wherein said data-input array comprises a touchpad.

28. The system of Claim 24, wherein each of said digital signals comprise a logic high digital signal.

29. The system of Claim 24, wherein at least one of said N passive devices comprises a diode.

30. The system of Claim 24, wherein at least one of said N passive devices comprises a resistor.

31. A method for scanning a switch array comprising:

a) sending a signal over a first I/O line of a plurality of N input/output (I/O) lines to a switch array comprising a maximum of N(N-1) input elements, wherein said plurality of N I/O lines are coupled to said input elements to create a plurality of unique signal paths, each of which uniquely couple two of said I/O lines through an associated input element;

b) receiving said signal over a second I/O line;

c) identifying an activated input element by determining which of said plurality of unique signal paths couples said first I/O line to said second I/O line through said activated input element.

32. The method of Claim 31, further comprising:

sequentially sending a plurality of output signals over said plurality of N I/O lines to scan said switch array.

33. The method of Claim 31, further comprising:

pulling each of said plurality of I/O lines to a logic low level to digitally distinguish those of said plurality of I/O lines driven to a logic high level by said signal.

34. The method of Claim 31, further comprising:

configuring said switch array so that between any pair of I/O lines two circuit paths exist, each defining a unique switch and passive device combination to differentiate between said two circuit paths.

35. The method of Claim 34, wherein in said unique switch and passive device combination, said passive device comprises a diode.

36. The method of Claim 31, wherein each of said maximum of N*(N-1) input element comprises a switch.

37. The method of Claim 31, wherein said switch array comprises a key matrix.

38. The method of Claim 31, wherein said switch array comprises an N*N matrix configured to support said maximum of N*(N-1) input elements.

39. The method of Claim 31, wherein said signal comprises a logic high signal.